MAHA BARATHI ENGINEERING COLLEGE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CEC 334 ANALOG IC DESIGN LAB MANUAL

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III Year/ V Semester B.E ECE

Regulation 2021

(As Per Anna University, Chennai syllabus)

CEC 334 ANALOG IC DESIGN LAB MANUAL

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4. DESIGN COMMON GATE AMPLIFIER AND ANALYZE ITS PERFORMANCE.

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1. DESIGN OF CMOS INVERTER AND ANALYZE ITS CHARACTERISTICS

AIM:

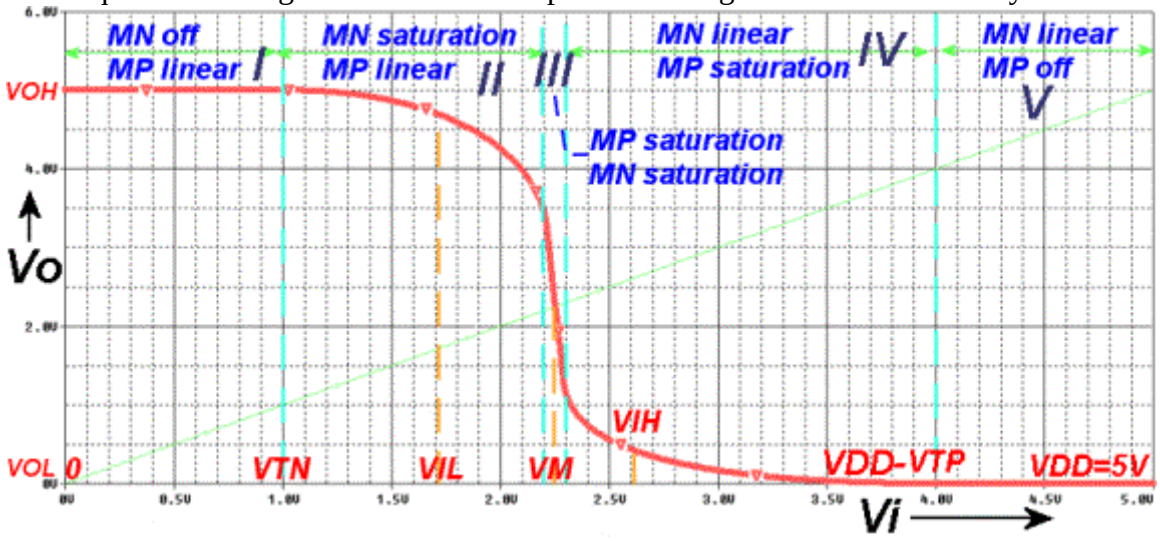
To Design of CMOS Inverter and analyze its characteristics using Tanner tools.

TOOLS REQUIRED:

- Tanner Tool
- Personal Computer

THEORY :

- A CMOS circuit is composed of two MOSFETs. The top FET (MP) is a PMOS type device while the bottom FET (MN) is an NMOS type. The body effect is not present in either device since the body of each device is directly connected to the device's source. Both gates are connected to the input line. The output line connects to the drains of both FETs.
- The MOSFETS must be perfectly matched for optimum operation, that is, they must have the same threshold voltage magnitude and conduction parameter.
- The drain current (ID) through the NMOS device equals the drain current through the PMOS device at all times. MOSFET gates have high input impedance and we assume the circuit's output sees no significant loading.
- VDD equals the voltage across the PMOS plus the voltage across the NMOS by KVL.



Region I

First we focus our attention on region I. In this case when we apply an input voltage between 0 and VTN. The PMOS device on since a low voltage is being applied to it. The NMOS is already negative enough and has no use for more free electrons so it refuses to conduct and turns into a large resistor. Since the NMOS device is on vacation, there is no current flow

through either device. VDD is available at the Vo terminal since no current is going through the PMOS device and thus no voltage is being dropped across it.

The PMOS device is forward biased (VSG > -VTP) and therefore on. This MOSFET is in the linear region (VSD<=VSG+VTP=VDD-Vo+VTP).

The NMOS device is cut off since the input voltage is below VTN (Vi=VGS<VTN).
The power dissipation is zero.

Region II

Here we raise the input voltage above VTN. We find that the PMOS device remains in the linear region since it still has adequate forward bias. The NMOS turns on and jumps immediately into saturation since it still has a relatively large VDS across it.

The PMOS device is in the linear region (VSD<=VSG+VTP).

The NMOS device is in the saturation region (Vi=VDS>=VGS-VTN=Vo-VTN).

Current now flows through both devices. Power dissipation is no longer zero.

The maximum allowable input voltage at the low logic state (VIL) occurs in this region. VIL is the value of Vi at the point where the slope of the VTC is -1. Put another way, VIL occurs at (dVo/dVi) =-1.

Region III

In the middle of this region there exists a point where Vi=Vo. We label this point VM and identify it as the gate threshold voltage. The voltage dropped across the NMOS device equals the voltage dropped across the PMOS device when the input voltage is VM. For a very short time, both devices see enough forward bias voltage to drive them to saturation.
The PMOS device is in the saturation region (VSD>=VSG+VTP=VDD-Vo+VTP).
The NMOS device is in the saturation region (VDS>=VGS-VTN=Vo-VTN).

Power dissipation reaches a peak in this region, namely at where VM=Vi=Vo.

Region IV

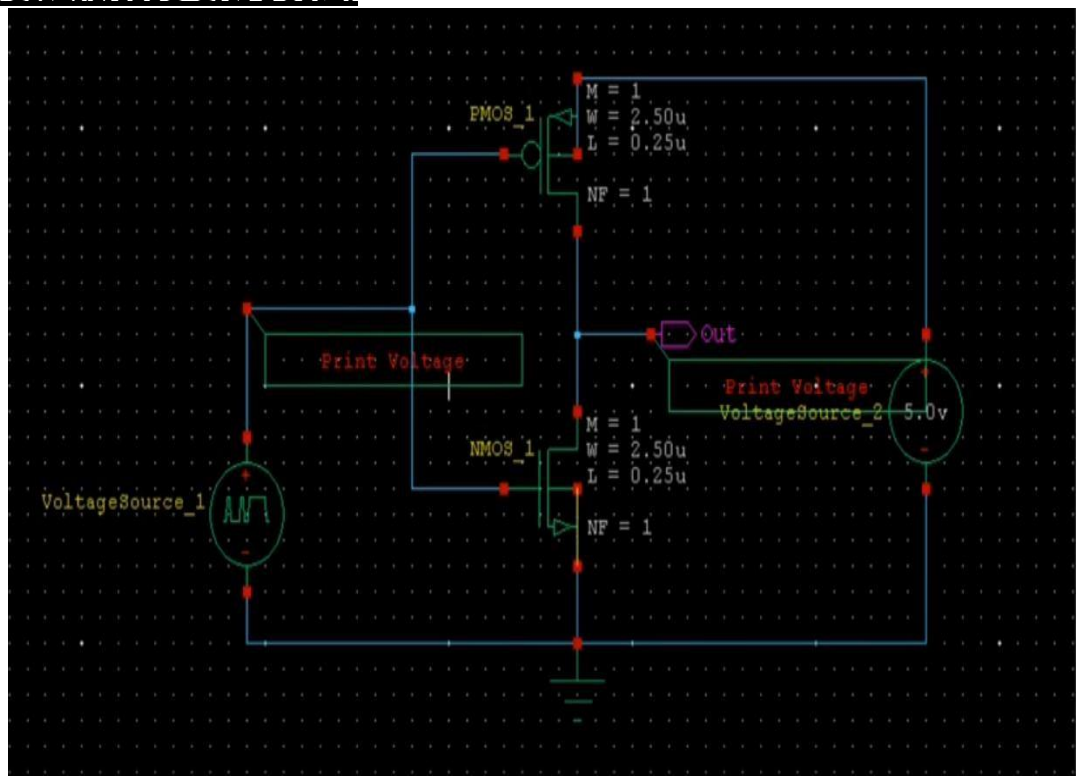
Region IV occurs between an input voltages slightly higher than VM but lower than VDD-VTP. Now the NMOS device is conducting in the linear region, dropping a low voltage across VDS. Since VDS is relatively low, the PMOS device must pick up the tab and drop the rest of the voltage (VDD-VDS) across its VSD junction. This, in turn, drives the PMOS into saturation. This region is effectively the reverse of region II.
The PMOS device is in the saturation region (VSD>=VSG+VTP=VDD-Vo+VTP).
The NMOS device is forward biased (Vi=VGS > VTN) and therefore on. This MOSFET is in the linear region (Vi=VDS<=VGS-VTN=Vo-VTN).
The minimum allowable input voltage at the logic high state (VIH) occurs in this region. VIH occurs at the point where the slope of the VTC is –1 (dVo/dVi)=-1.

Region V

The NMOS wants to conduct but its drain current is severely limited due to the PMOS device only letting through a tiny leakage current. The PMOS is out to lunch since it is seeing a positive drive but it is already positive enough and has no use for more. This drain current let through by the PMOS is too small to matter in most practical cases so we let ID=0. With this information we can conclude that VDS=Vo=0 V for the NMOS since no current is going through the device. We have, in effect, sent in VDD and found the inverter's output to be zero volts. For CMOS inverters, VOH=VDD. VOL is defined to be the output voltage of the inverter at an input voltage of VOH. We have just proven that VOL=0.
The PMOS device is cut off when the input is at VDD (VSG=0 V).

The NMOS device is forward biased (Vi=VGS > VTN) and therefore on. This MOSFET is in the linear region (Vi=VDS<=VGS-VTN).
The total power dissipation is zero just as in region I.

SCHEMATIC CAPTURE:



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Procedure:

1) Start S-Edit

- Create a new design
- Add the Tanner_Projects\Libraries\All\All.tanner library to the library list on the left
- Create a new Cell called “TOP” using the Pull Down Menus
- Cell - New View Name = TOP View Type = schematic - Setup the simulation using the Pull Down Menus
- Setup – SPICE Simulation
- Highlight the General Tab of the Setup SPICE window and set the following:
  SPICE File Name: Enter file name
  Library Files: ..\Generic_025_Kit\Generic_025_SPICE_Models_Level1.lib
  Simulation Results File Name: Enter File Name
- Check the “Transient/Fourier Analysis” box on the left and set the following: Stop Time = 2ns Maximum Time Step = 10ps - Click “OK”

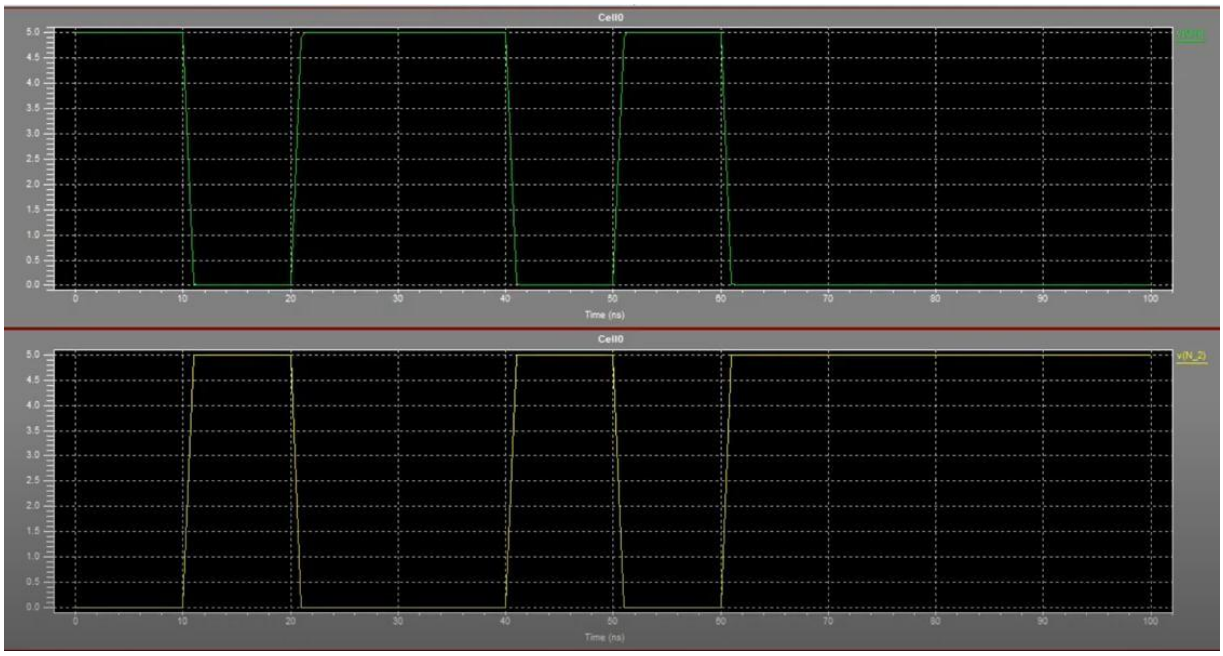
2) Create the Inverter

a) Create a new schematic view using the pull-down menus: - Cell - New View Name = Inverter View Type -schematic

b) Enter the inverter schematic: - Entering the NMOS: Name = M1, L = 0.25u, W = 2.5u, Model =NMOS

- Entering the PMOS: Name = M2 L = 0.25u W = 5.0u Model =PMOS
- Entering the Ports: Ports are entered using the icons on the top of the S-edit window.
- Enter the following:
    In Port: Name it “IN” Out Port: Name it “OUT”
    In/Out Port: Name it “VDD”
    In/Out Port: Name it “VSS”
- Wire up the Inverter Enter wire connections as shown in the previous figure
- For Simulation:
    a) First, check you design using the pull down menus:
    - Tools – Design Checks (any warnings or errors will be shown at the bottom)
    b) Simulate your design:
- Clock on the Green Arrow to start the simulator:
-The T-Spice window will appear. If everything is OK, the waveform viewer will also appear.
-If everything worked, your waveforms should look like simulation results.

SIMULATION RESULTS:



RESULT:

Thus the cmos inverter was designd and analyze its characteristics are successfully executed and output is verified.

2. DESIGN A COMMON SOURCE AMPLIFIER AND ANALYZE ITS PERFORMANCE

AIM:

To design and simulation of Common source amplifier and analyze its performance using Tanner tools.

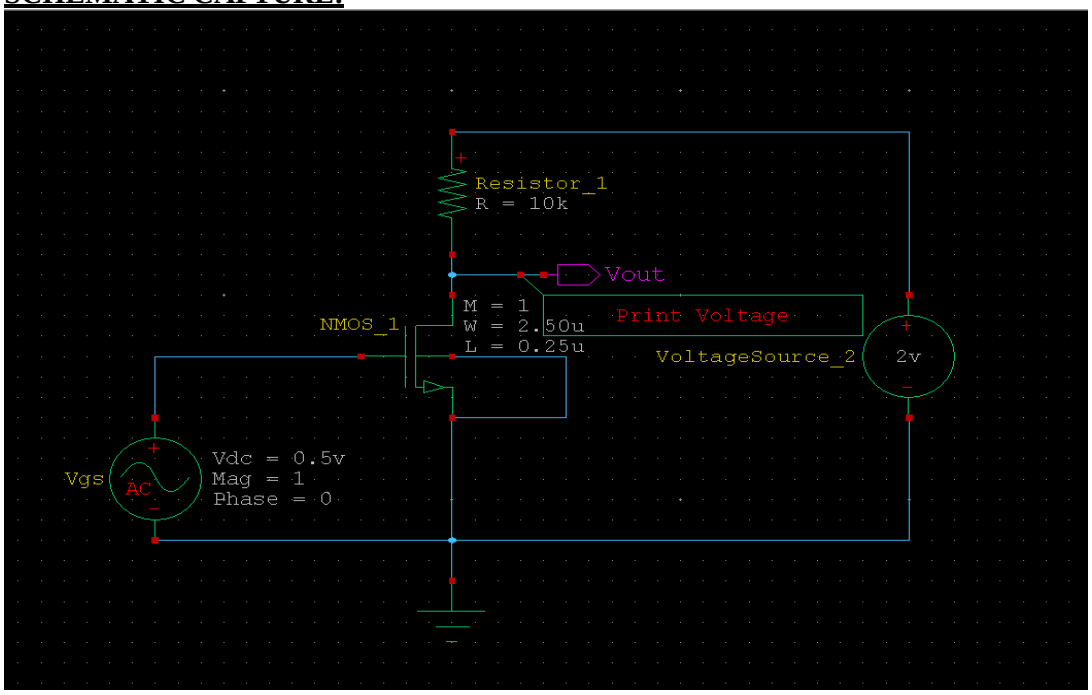
TOOLS REQUIRED:

- Tanner Tool
- Personal Computer

THEORY:

Common Source (CS) structure is the very basic form of an amplifier using MOSFETs.Though it is simple, it gives a decent gain - bandwidth product. Design of CS amplifier isfirst step for any analog circuit beginner. however the gain depends on Rc resistor. To have a large gain, Rc must be large but large Rc makes VD smaller hence MOSFET may slip into triode region. So instead of Rc if we put a device which offers high resistance for small signal and low voltage drop for DC, we can achieve relatively large gain. We use a PMOS transistor in saturation region as an active load which offers high resistance for small signal and low voltage drop (V_{DS}) for DC. The active load is biased using current mirror technique.M1 is the transistor in CS configuration,M2 is active load and M3 is a diode connected transistor which mirrors I_{ref} current into M2 transistor. Since drain and gate of M3 are tied together, it offers a good bias stability

SCHEMATIC CAPTURE:



PROCEDURE:

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- Check the “Transient/Fourier Analysis” box on the left and set the following: Stop Time = 2ns Maximum Time Step = 10ps - Click “OK”

2) For Simulation

a) First, check you design using the pull down menus:

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b) Simulate your design:

- Clock on the Green Arrow to start the simulator:

-The T-Spice window will appear. If everything is OK, the waveform viewer will also appear.

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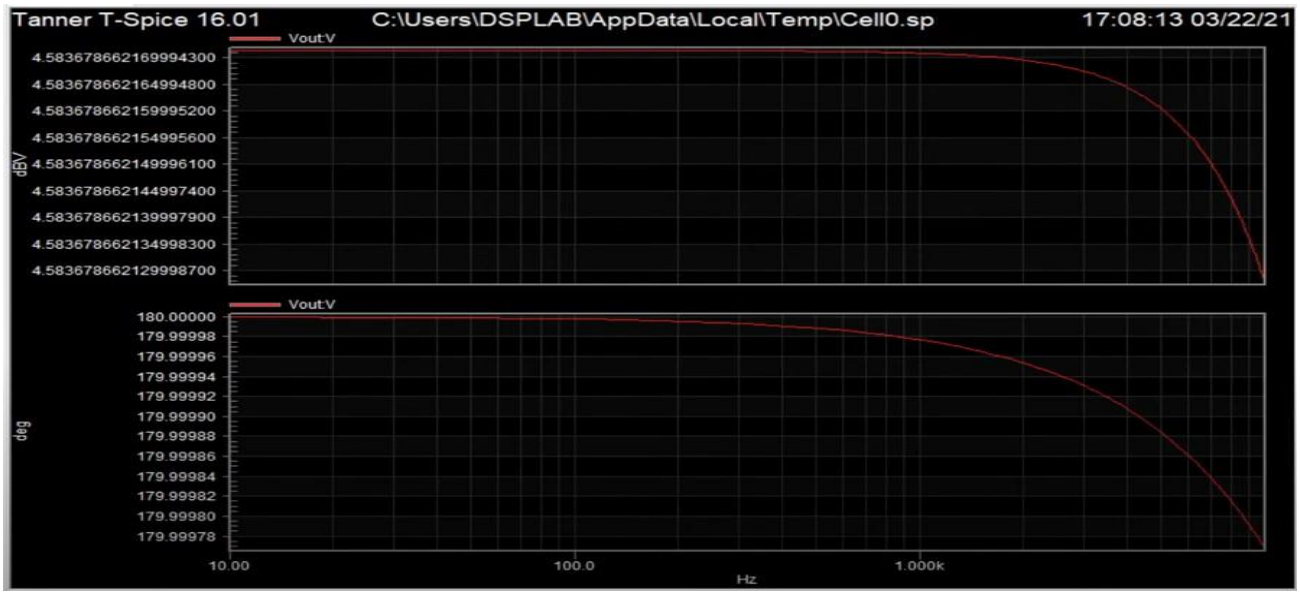
SIMULATION RESULTS:



RESULT:

Thus the common source ampilfier was designed and its performance are successfully executed andoutput is verified.

3. DESIGN A COMMON DRAIN AMPLIFIER AND ANALYZE ITS PERFORMANCE

AIM:

To design a common drain amplifier and analyze its performance using Tanner tool..

TOOLS REQUIRED:

- Tanner Tool
- Personal Computer

THEORY:

The common drain (CD) amplifier, also known as the source follower, is a type of MOSFET amplifier configuration.

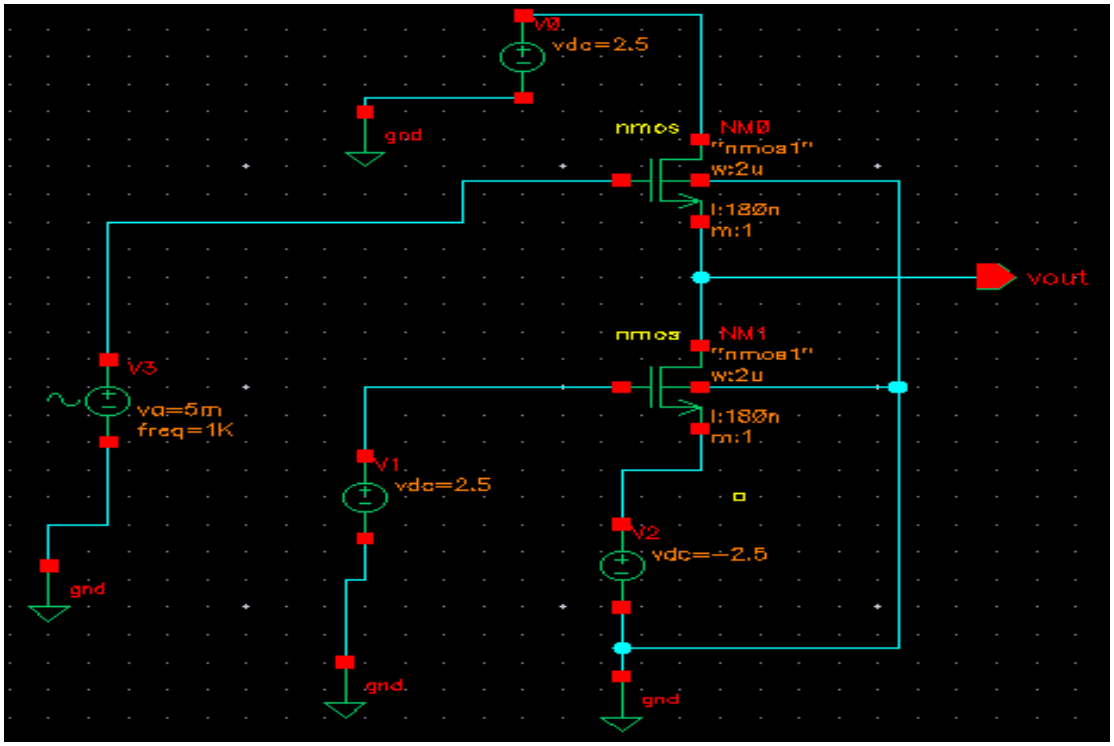
In a CD amplifier, the input signal is applied to the gate terminal, and the output is taken from the source terminal.

- **Configuration:** In a common drain amplifier, the MOSFET transistor is configured in a way that the source terminal is common to both input and output signals.
- **Operation:** The input signal is applied to the gate terminal, modulating the conductivity of the channel. As the input voltage varies, the output voltage follows the input voltage with some attenuation.
- **Voltage Gain:** The voltage gain of the common drain amplifier is less than unity (typically slightly less than 1). This is because the output voltage is taken from the source terminal, which has a voltage drop due to the MOSFET's channel resistance. The gain can be expressed as $Av \approx 1 - gm * Rd$, where gm is the transconductance of the MOSFET and Rd is the load resistor connected to the drain terminal.

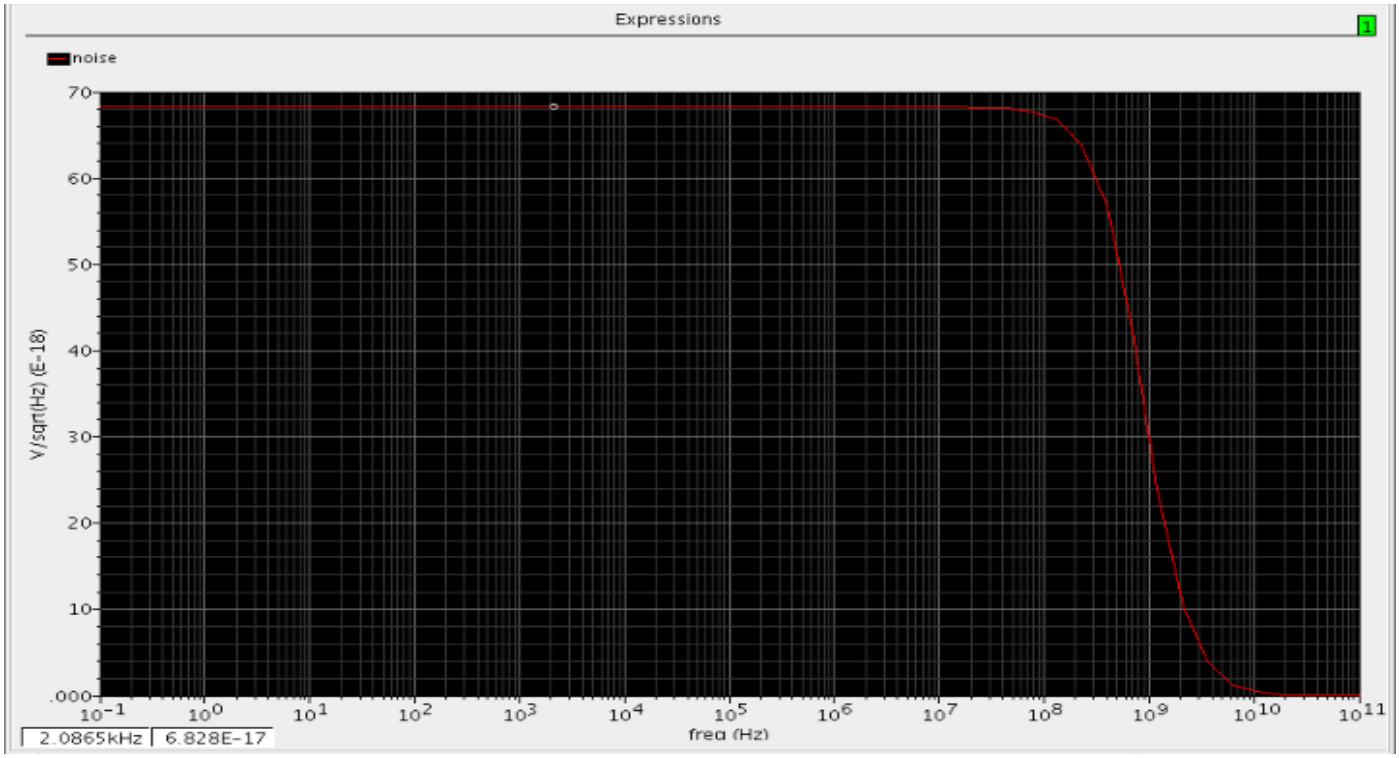
Characteristics:

- **High Input Impedance:** The input impedance of the CD amplifier is mainly determined by the gate-source capacitance of the MOSFET transistor and is typically very high.
- **Low Output Impedance:** The output impedance of the CD amplifier is primarily determined by the output resistance of the MOSFET transistor and is typically low.
- **Voltage Following:** The output voltage follows the input voltage with a slight voltage drop due to the voltage-divider effect caused by the MOSFET's channel resistance.
- **Low Voltage Gain:** The voltage gain of the CD amplifier is slightly less than unity due to the voltage-divider effect.
- **High Linearity:** The CD amplifier exhibits high linearity due to the absence of feedback from the output to the input.

SCHEMATIC DIAGRAM:



SIMULATION RESULT:



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RESULT

Thus the common drain ampilfier was designed and its performance are successfully executed andoutput is verified.

4. DESIGN A COMMON GATE AMPLIFIER AND ANALYZE ITS PERFORMANCE

AIM:

To design a common gate amplifier and analyze its performance using Tanner tool..

TOOLS REQUIRED:

- Tanner Tool
- Personal Computer

THEORY:

In common source amplifier and source follower circuits, the input signal is applied to the gate of a MOSFET. It is also possible to apply the input signal to the source terminal by keeping common gate terminal. This type of amplifier is called as common gate amplifier.
the CG amplifier in which the input signal is sensed at the source terminal and the output is produced at the drain terminal. The gate terminal is connected to V_B i.e. dc potential which will maintain the proper operating conditions.

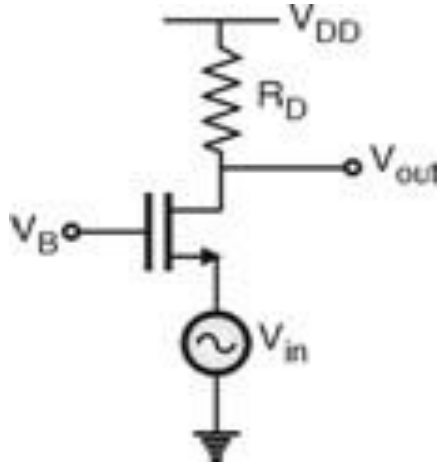
By analizing the small signal equivalent circuit, the voltage gain of CG amplifier is given by,

$A_v = = g_m R_D$

The important point is the gain is positive, further the input impedance is given by which shows that the input impedance of common gate amplifier is relatively low. Furthermore, the input impedance of of common gate stage is relatively low only if the load resistance connected to the drain is small.

SCHEMATIC DIAGRAM:

Schematic Diagram



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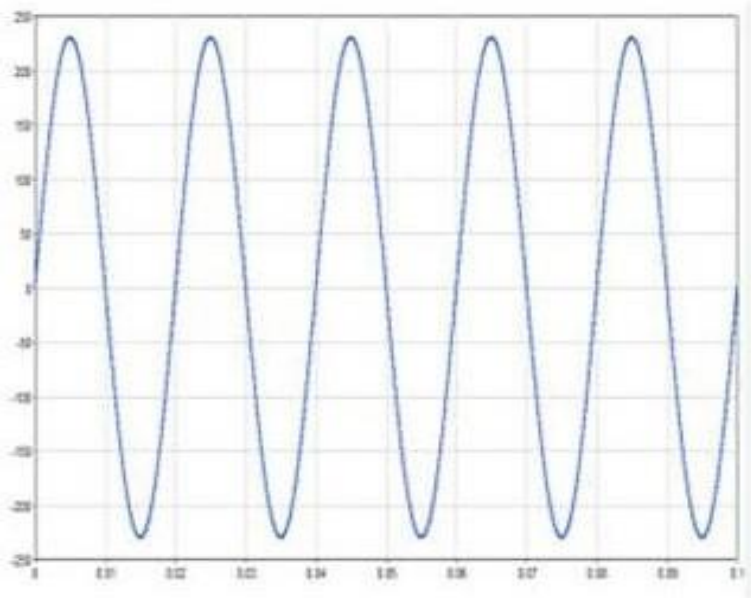
Schematic output



RESULT

Thus the common gate ampilfier was designed and its performance are successfully executed andoutput is verified.

5. DESIGN A DIFFERENTIAL AMPLIFIER WITH RESISTIVE LOAD USING TRANSISTORS

AIM:

To design differential amplifier using Tanner tools.

TOOLS REQUIRED:

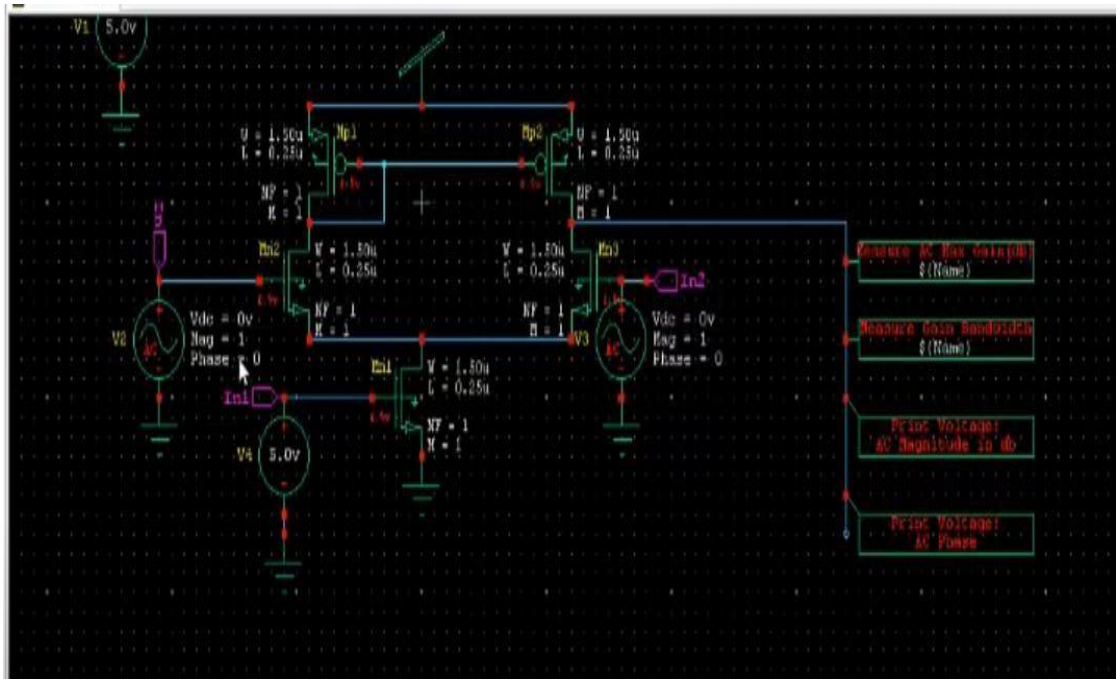
- Tanner Tool
- Personal Computer

THEORY:

A difference amplifier is a circuit that gives the amplified version of the difference of the two inputs, $Vo = A(V_1-V_2)$, Where V_1 and V_2 are the inputs and A is the voltage gain.
Here input voltage V_1 is connected to non-inverting terminal and V_2 to the inverting terminal.
This is also called as differential amplifier. Output of a differential amplifier can be determined using super position theorem.
When $V_1=0$,
the circuit becomes an inverting amplifier with input V2 and the resulting output is $V_{02}= -Rf /Ri (V2)$.
When $V_2=0$,
the circuit become a non-inverting amplifier with input V1 and the resulting output is $V_{01}= Rf/Ri(V1)$.
Therefore the resulting output according to super position theorem is

$$V_o = V_{01} + V_{02} = R_f/R_i(V_1-V_2)$$

SCHEMATIC CAPTURE:



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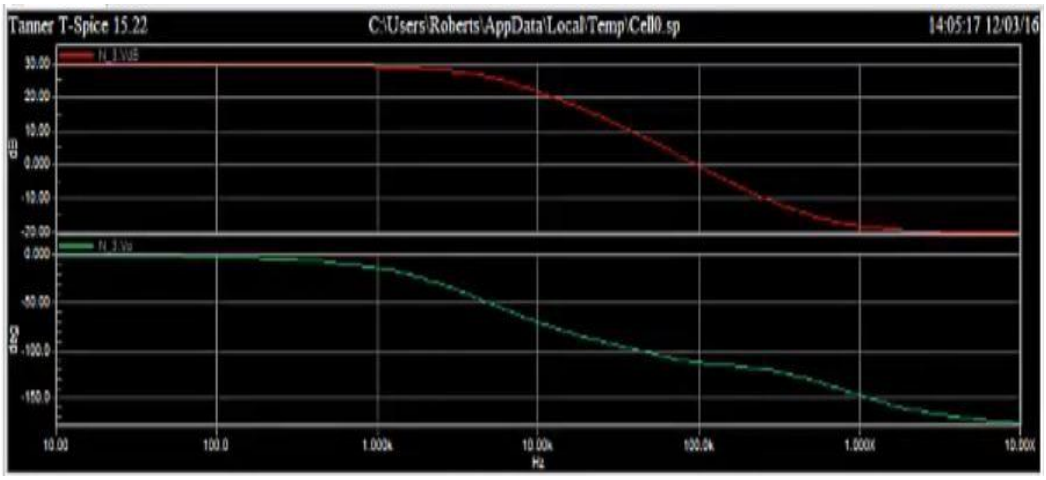
SIMULATION RESULTS:



RESULT:

Thus the differential amplifier was designed and its characteristics are successfully verified and output executed..

6. DESIGN THREE STAGE AND FIVE STAGE RING OSCILLATOR CIRCUIIT

AIM:

To design three stage and five stage ring oscillator circuit and compare its frequencies using tanner tool.

TOOLS REQUIRED:

- Tanner Tool
- Personal Computer

THEORY:

Ring oscillator is cascaded combination of odd number of delay stages, connected in a close loop chain with a unity gain negative feedback. The ring oscillators are designed with a chain of delay stages have created great interest because of their numerous useful features. These attractive features are: (i) It can be easily designed with the state-of-art integrated circuit technology (CMOS, BiCMOS), (ii) It can achieve its oscillations at low voltage, (iii) It can provide high frequency oscillations with dissipating low power, (iv) It can be electrically tuned, (v) It can provide wide tuning range and (vi) It can provide multiphase outputs because of their basic structure. These outputs can be logically combined to realize multiphase clock signals, which have considerable use in a number of applications in communication systems. Fig.1. Hardware structure of single ended inverter based ring oscillator. In the ring oscillator circuit, the feedback from its last output to the input causes the oscillations as shown in Fig.1. Odd number of inverter stages used to give the effect of single inverter amplifier with a negative feedback gain of greater than 1 so that the output will be in opposite direction to the input. Ring oscillator needs only a power to operate above the threshold voltage and then the oscillations starts spontaneously.

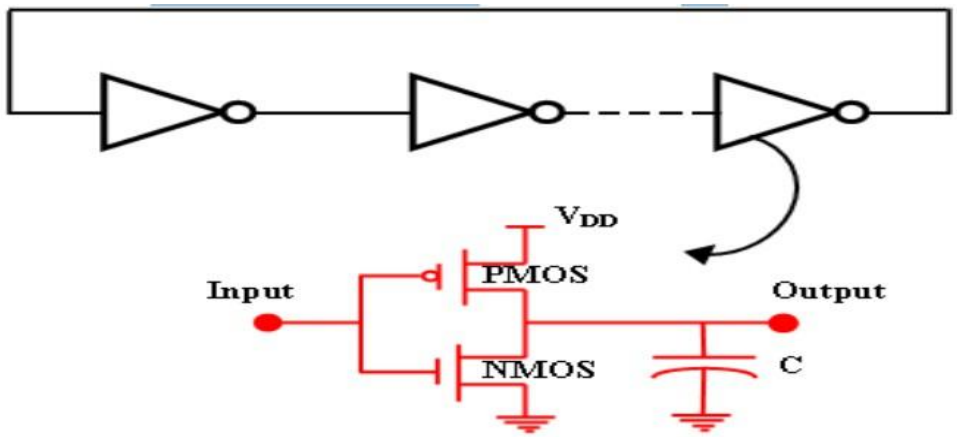
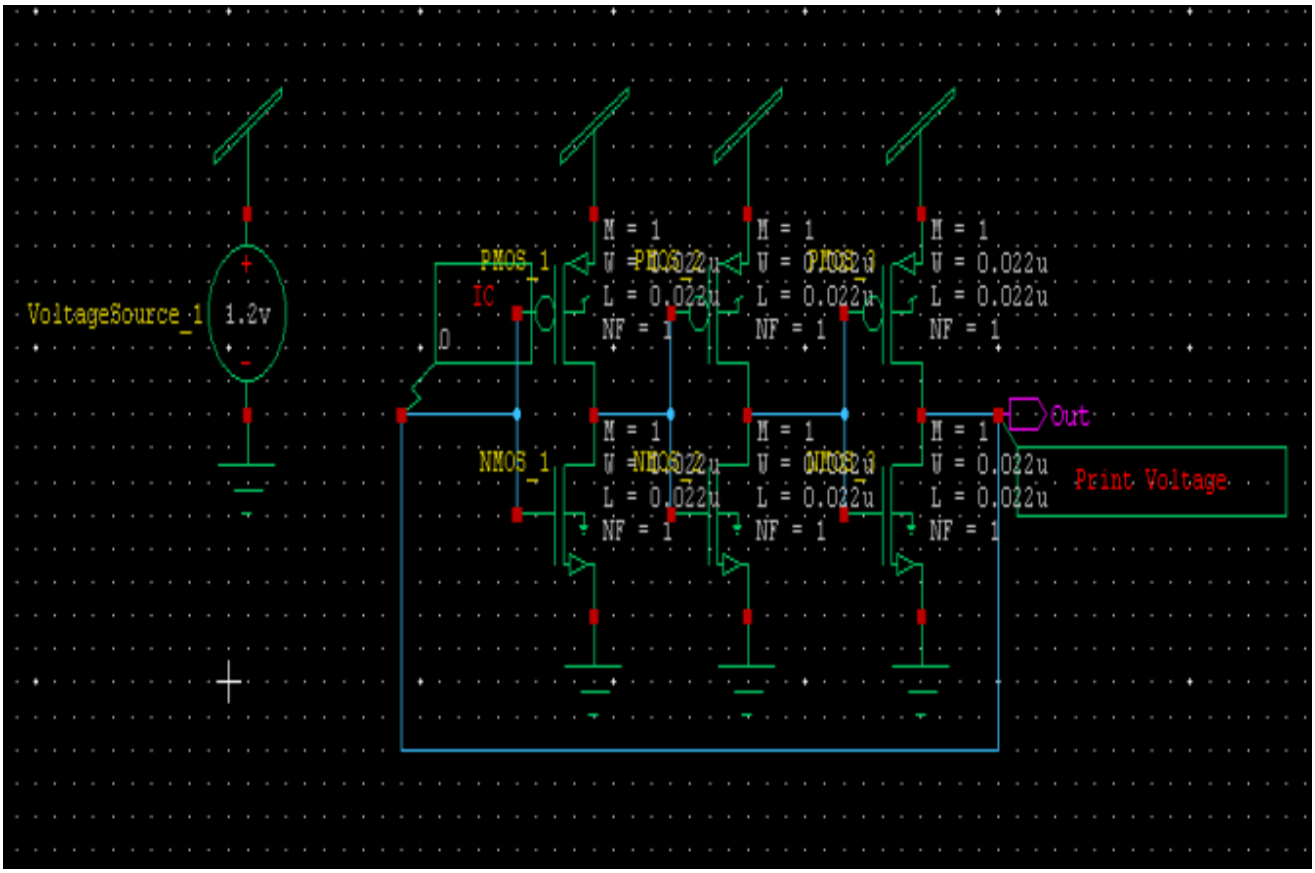


Fig.1. Hardware structure of single ended inverter based ring oscillator.

To achieve self-sustained oscillations, the ring must provide a phase shift of 2π and have unity voltage gain at the frequency of oscillation. In an N-stage ring oscillator, each stage provides a phase shift of π /N and dc inversion provides the remaining phase shift of π. Therefore, the oscillating signal must go through each of the m delay stages once to provide the first π phase shift in a time of N td and it must go each stage a second time to obtain the remaining phase shift in a time period of 2N td. Thus the frequency of oscillation is given by: (1) Where, is the oscillation frequency of the ring oscillator, is the propagation delay of each delay stage and N is the number of stages. The oscillation frequency of a ring oscillator depends on the propagation delay td per stage and the number of stages used in the ring structure. The oscillation frequency of a ring oscillator may be determined from the expression of td which depends on the circuit parameters. But the main difficulty in obtaining the expression of td arises due to the nonlinearities and parasitics of the circuit.

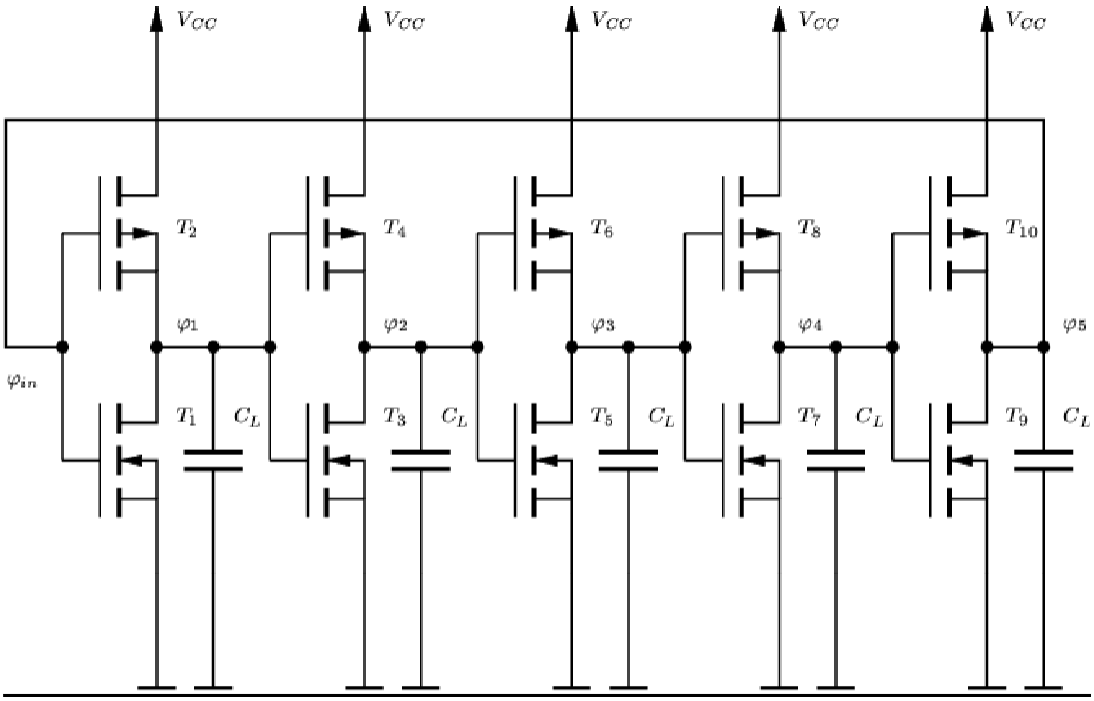
SCHEMATIC DIAGRAM:

THREE STAGE RING OSCILLATOR:



Thus the differential amplifier was designed and its characteristics are successfully verified and output executed..

FIVE STAGE RING OSCILLATOR:



SIMULATION RESULT:

THREE STAGE RING OSCILLATOR

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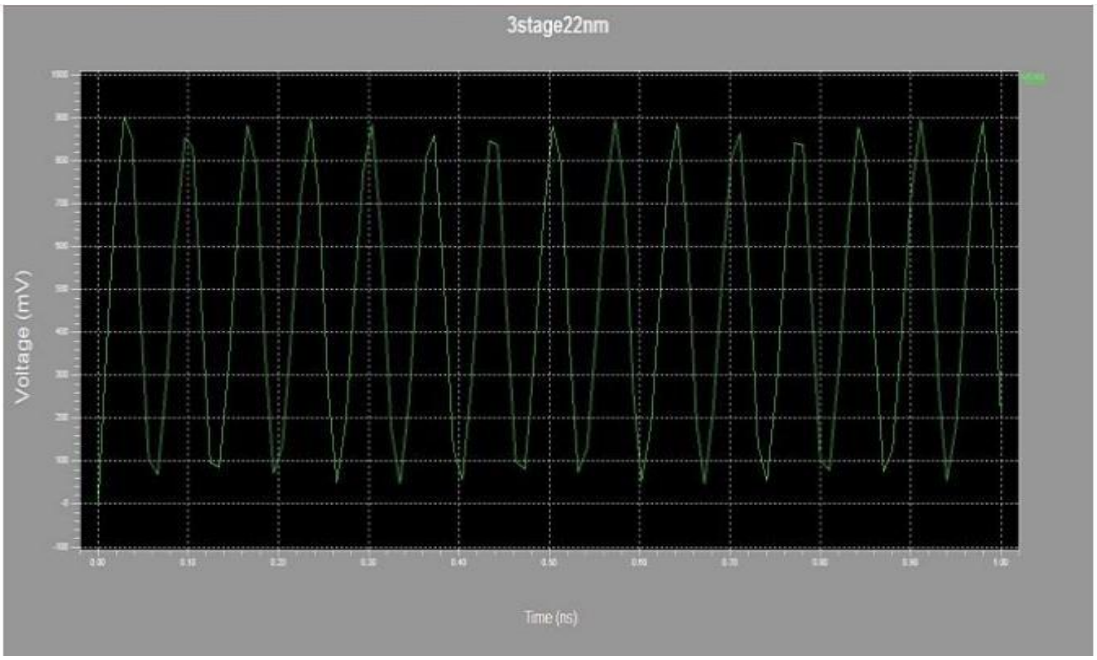

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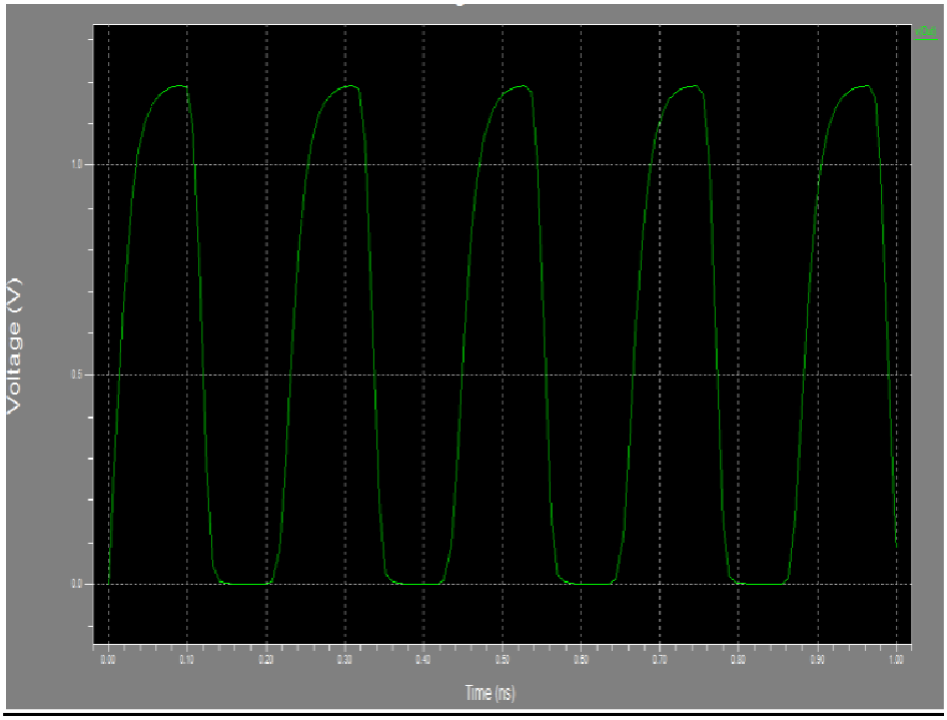
FIVE STAGE RING OSCILLATOR



PROCEDURE:

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b) Simulate your design:
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-If everything worked, your waveforms should look like simulation results.

RESULT:

Thus the three stage and five stage ring oscillator was designed and its characteristics and output executed successfully.